SM16716

Description

The SM16716 is a constant current driver designed for LED decorative lighting and point lamp application, which provides 3-channel constant current drive and PWM output, especially suitable for discrete, multi-gray scale full-color lighting system.

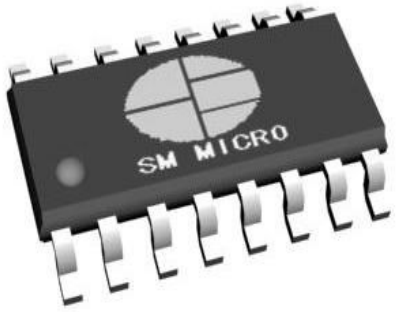
Feature

- 3-channel open-drain output, maximal current: 60mA
- Maximal withstand voltage of OUT: 26V
- Patented PCCM constant current output drive technology, constant current precision: <±5%
- Built-in LDO circuit, VDD range: 3.3-6.0V
- Double line self-reshaping data transmission, maximum clock: 30Mhz
- 256 gray level, 8 bits gray data
- Package：SOP16
- ESD HBM：>4KV

Application

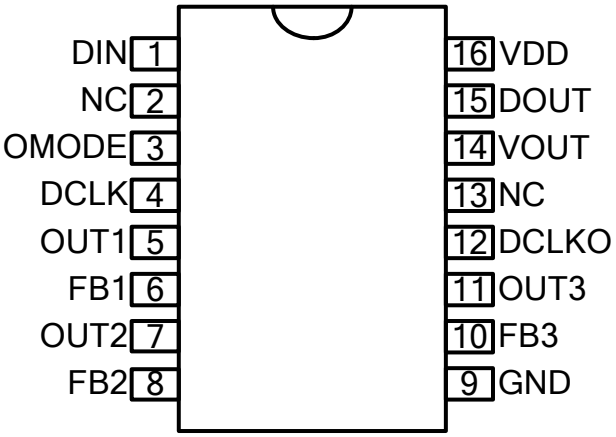
- Interior LED decorative lighting
- Exterior LED lighting of building
- Wash wall lamp, curtain screen
- Luminous character, guardrail tube

Package Diagram

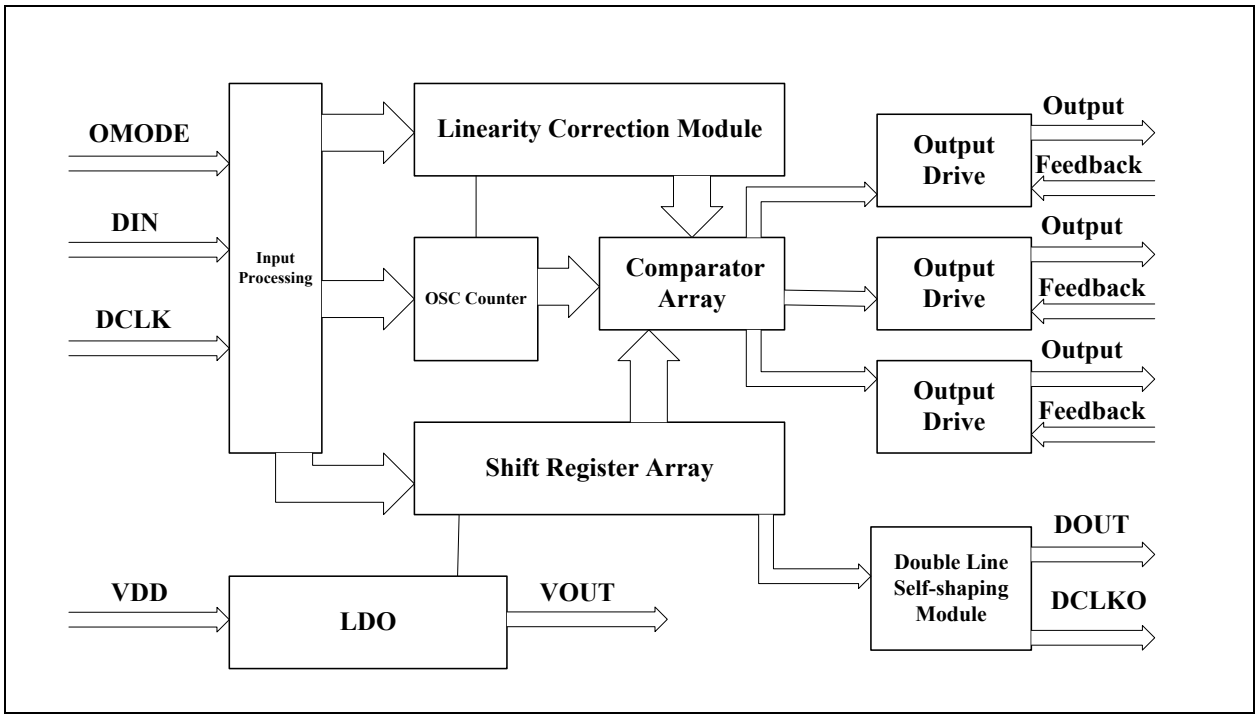


SOP16

Pin Definition



Internal Block Diagram



Pin Description

Symbol	Pin Name	Pin No.	Description
DIN	Data Input	1	Displayed data input port
NC	No connection	2,13	No connection
OMODE	Set polarity port	3	Control of the output polarity: OMODE=I(default), output mode: interior constant current/constant voltage drive; OMODE=0, plug-in driving mode. Built-in pull-up resistor
DCLK	Clock input	4	Clock input of the serial data, built-in pull-up resistor
OUT1，OUT2，OUT3	Drive output	5,7,11	Three-line driving output
FB1，FB2，FB3	Feedback input	6,8,10	Under CCM, current setting port of the three-line output
GND	Ground	9	Ground
DCLKO	Clock input	12	Serial clock input, regenerate through the interior PLL
VOUT	LDO output voltage	14	LDO output voltage
DOUT	Data output	15	Serial data output, strong driving output
VDD	Chip power	16	5V±10%

Electric Parameter

Absolute Maximum Parameter（Ta = 25℃）

Parameter	Symbol	Range	Unit
Logic power& voltage	VDD	-0.5——+6.0	V
Withstand voltage of the output port	V_{OUT}	0——26	V
Logic input voltage	V_{I1}	-0.5——VDD+0.5	V
Output current of the OUT drive	I_{OL1}	0——60	mA
Current error between channels	$\%dI_{OUT}$	Between channels<±5%，between chips<±5%	%
Power dissipation	PD	600	mW
Operating temperature	T_{OPT}	-20——+80	℃
Storage temperature	T_{STG}	-40——+150	℃

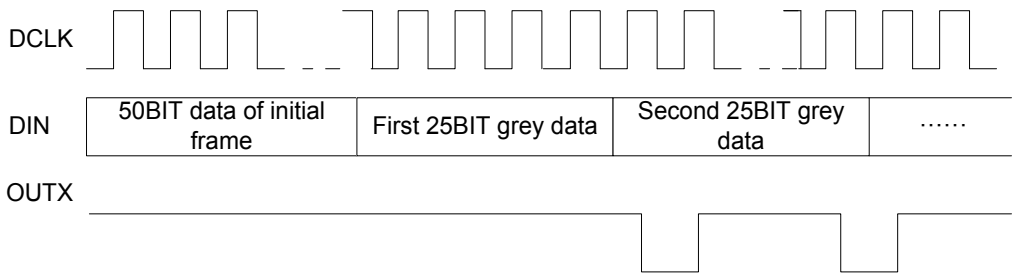
Electric Parameter（Ta = 25℃）

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Quiescent current	IDD			0.8	mA	The load capacitor of the VOUT port: 0.1uF，VDD = 5.0V
Power dissipation	P_{out}			350	mW	
VDD voltage	VDD	3.3	5.0	7.0	V	
VOUT voltage	V_{OUT}	4.5	5.0	5.5	V	VDD = 6.5V
Withstand voltage of the OUT port	$V_{DS,MAX}$			26	V	
Input voltage of high level	VIH	0.7*VDD	—	VDD	V	
Input voltage of low level	VIL	0	—	0.3*VDD	V	
Drive current of DOUT/DCLKO	I_{OH}	-50	-60	-70	mA	VDD = 5.0V
	I_{OL}	50	60	70	mA	
Voltage of FB1~3	V_{FB}	0.68	0.75	0.82	V	OMODE = 1
Interior CCM OUT1~3 current	I_{OUT}	33.75		41.25	mA	FB resistor = 20Ω
		14.55		17.78	mA	FB resistor = 40Ω
OUT1~3 leakage current	LEAKAGE_OUT			1	uA	VDD = 5.0V，The input data of DIN are all 0
Interior PWM clock frequency	f_{OSC}		1.03		MHz	VDD = 5.0V

Timing Sequence（Ta = 25℃）

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Data clock frequency	f_{CLK}	—		30	MHz	
Clock high-level width	T_{CLKH}	30	—	—	ns	
Clock low-level width	T_{CLKL}	30	—	—	ns	
Clock setup time	T_{SETUP}	10	—	—	ns	
Dara hold time	T_{HOLD}	5	—	—	ns	
Delay time of cascade output signal	T_{PD}			12	ns	CL=30pF,RL=1K
Minimal PWM opened width	T_{OMIN}	250			ns	I_{OUT}=30mA
Maximal opened time the driving outputs	T_{ON}			80	ns	I_{OUT}=20mA
Maximal closed time the driving outputs	T_{OFF}			80	ns	I_{OUT}=20mA

Function Description



1. Shift in 50Bits ‘‘0’’ to be the initial frame at first, and then shift in every data frame. The initial frame and the data frame are shifted in MSB first. Every data bit is shifted in at the rising edge of DCLK.
2. The first data frame corresponds to the closest LED light, the format includes the initial bit of 1Bit ‘‘1’’ and three sets of 8Bits gray data;
3. When all the data of the chip are transferred, transfer extra DCLK pulse counts which correspond to the number of the chip, and the above data starts to take into effect. The data signal of the extra DCLK pulse counts transferred is low –level. (The data signal issues ‘‘0’’, and the clock signal issues based on the above format);
4. Every set of the gray data is composed with the 1Bit“1”+24Bit gray data.

- The Cascade Connection of the Signal

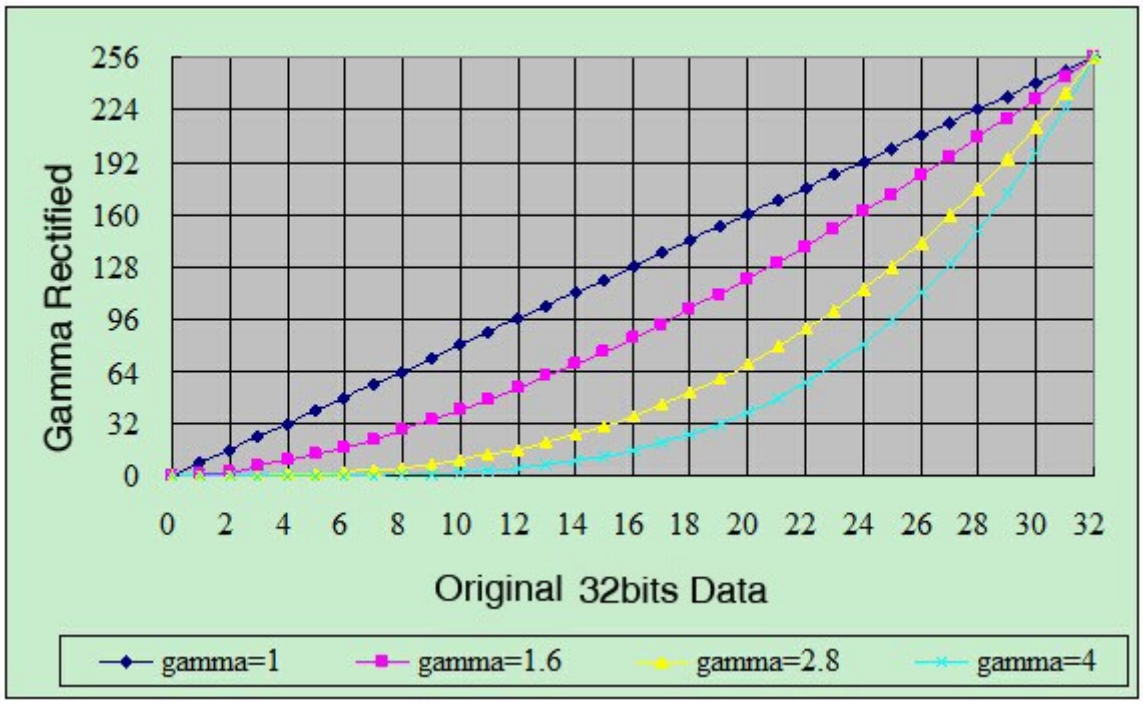
  In the application, transport distance of the cascade connection of the chip could be long. The transport protocol adopts the double-line transport protocol that self-adjusts the signal, it can eliminate the race hazard between the clock signal and the data signal. In addition, the DOUT and DCLKO design the push-pull driving circuit. A 6-meter long signal line can be driven when the clock is at 2MHz, which is verified in the test. To avoid signal reflection, a resistor (50Ω) should be cascaded between DOUT/DCLKO of one chip and DIN/DCLK of another.

- 256-level Linear PWM Output

  The chip adopts 8-bit, 256-level PWM output protocol.

  By the reason of the adoption of the signal self-reshaping double-line transport protocol, the chip supports high-speed data transportation. In the application, it can be applied to play the video. However, this kind of application presents high requirement to the gray level. The 256-level gray of the chip enables good demonstration.

  If the displayed source data is a <8-bit data, then the gamma correction can be conducted through the controlling system.

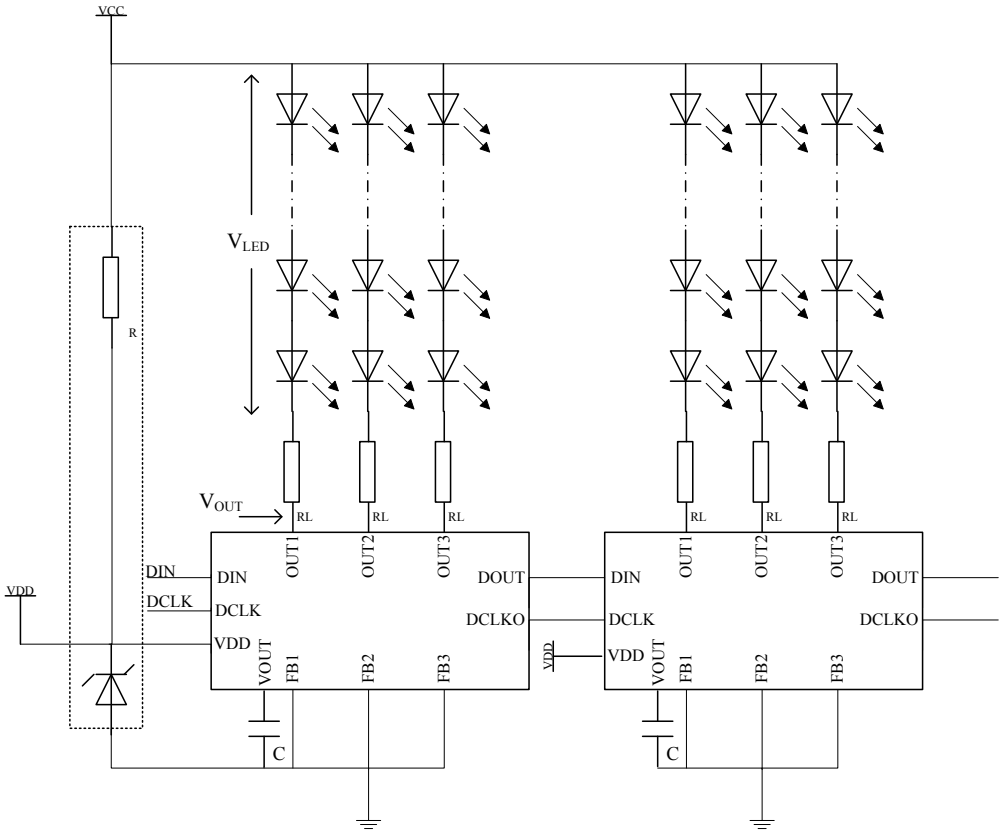


Original 32bits, Gamma-corrected Data Diagram

When the gamma rectification is done, the display effect will be better without gray. Contact the controlling system supplier about the specific gamma correction.

Typical Application

- Internal Constant Voltage Driving Mode



The mode is applied in the conditions when the power VCC is less than 12V and every current is less than 40mA. If VCC≤7.0V, the circuit in the dashed box can be saved (refer to the above diagram) and the VDD of the chip can be connected directly to the external power VCC.

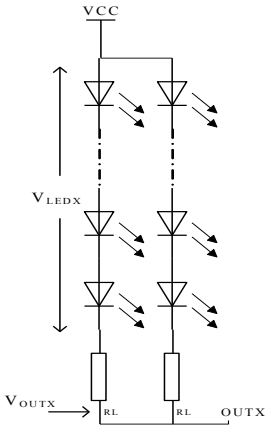
Regulated resistor of the current:： $RL = (VCC—V_{LED}—V_{OUT})/I_{LED}$

RL is the current-limiting resistor, VCC is the supply voltage of the LED light, V_{LED} is the sum of forward voltage drop of all the LED lights, V_{OUT} is the saturation drop-voltage (about 0.4~0.8V) conducted by the output to the ground, I_{LED} is the operating current of the LED, which is below 20mA normally.

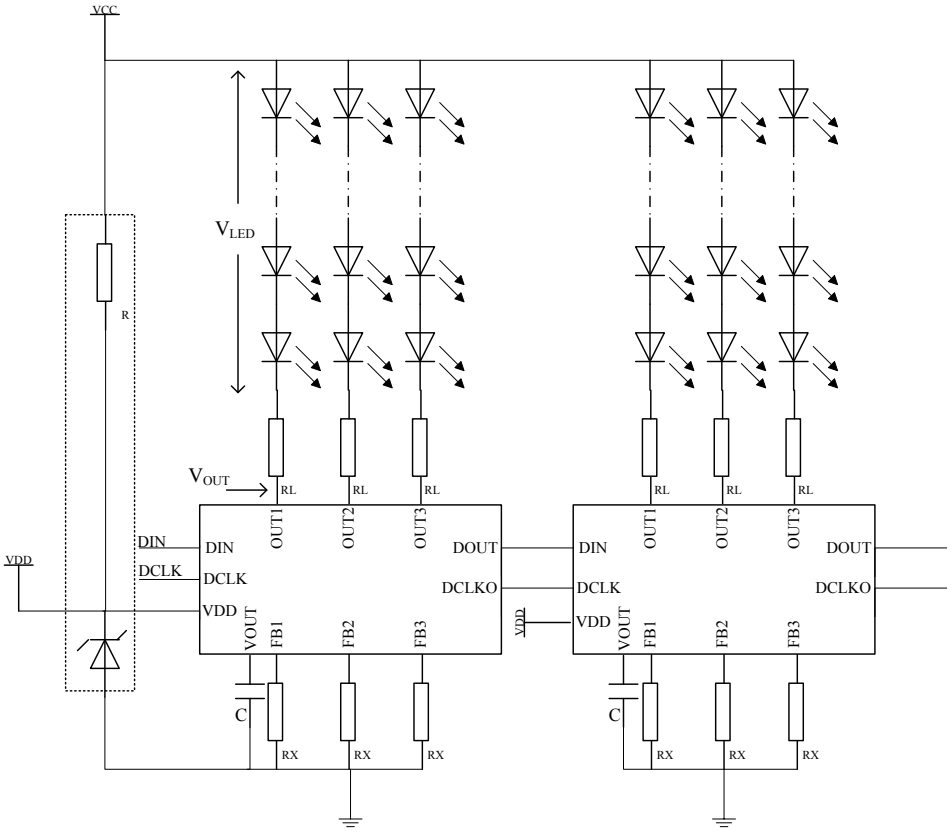
The driving capability of SM16716 is strong; the connection method of “series-parallel” can be adopted in some application with multi-LEDs. As it’s known in the diagram at the right side, the dissipation power PD must not exceed the ultimate value.

$PD=I_{LED1}*V_{OUT1}+I_{LED2}*V_{OUT2}+I_{LED3}*V_{OUT3}+PIC$

PIC is the basic power consumption of the IC, which is below 25mW normally.



- Built-in Constant Current Mode



The situation that the mode (OMODE=High Level or Opened) adapts is essentially the same as the internal constant voltage driving mode. The only difference is that there is a current regulator RX at the FB1~3 port, and the current through the LED is determined by RX:

$$I_{LED} = V_{FB}/RX \ (V_{FB} = 0.75V)$$

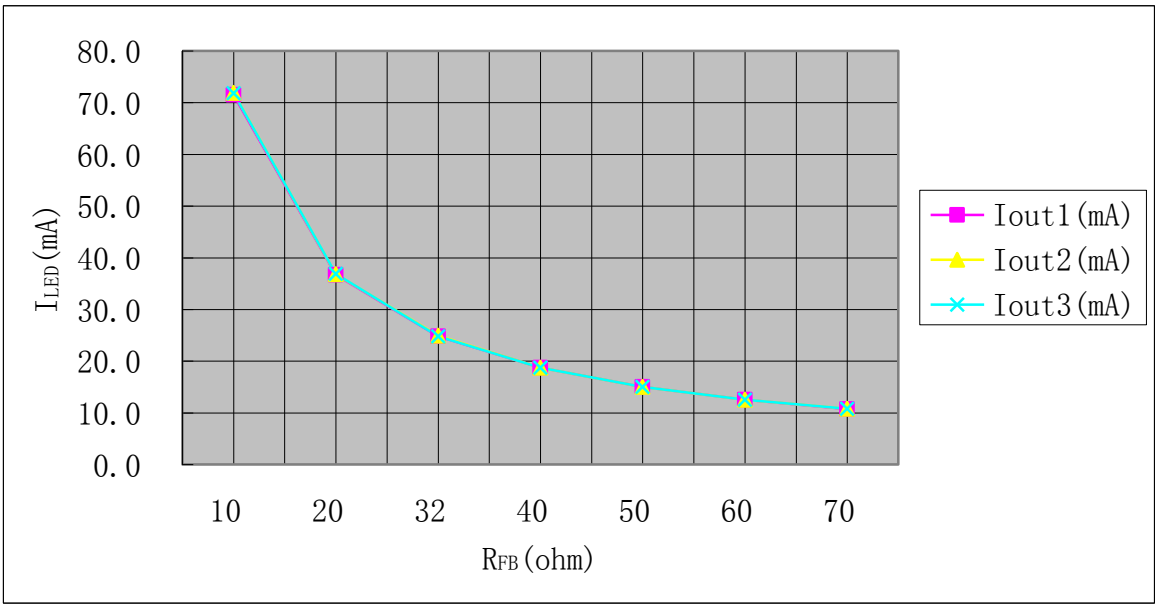


Diagram 1 I_{LED}—R_{FB} Curve

Attention: After the breakover, the constant current condition can be maintained under the circumstance that the voltage of the OUT port to the ground should be 1.5V~15V, namely,

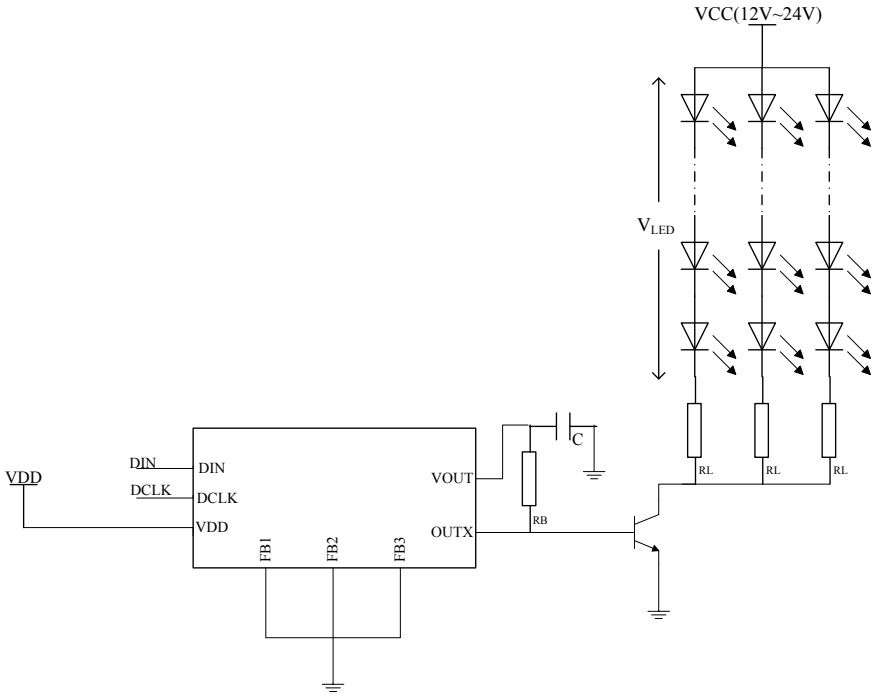
V_{LED}+15V+I_{LED}*RL≥VCC≥V_{LED}+1.5V+ I_{LED}*RL

The dissipation power PD cannot exceed the ultimate value in the parameter selection of the circuit:

PD=I_{LED1}*(V_{DS1}-0.75V) + I_{LED2}*(V_{DS2}-0.75V) + I_{LED3}*(V_{DS3}-0.75V) + PIC

The I_{LED1}, I_{LED2}, I_{LED3} are the value of the current that flow through each LED lamp, V_{DS1}, V_{DS2}, V_{DS3} are the voltage of each output to the ground. Normally, the value of RL is dozens of ohm, which shows no influence to the I_{LED}, and it can be ignorable. However, a proper value of RL contributes to the reduction of the wasted power PD of the chip, and the stability of the chip can be improved.

- Plug-in Constant Voltage Mode



This mode (OMODE=ground connection) can be applied in the conditions of multi-LED lamps or higher voltage, in fact, it controls the external NPN power BJT to drive multi-LED lamps through the OUTX output.

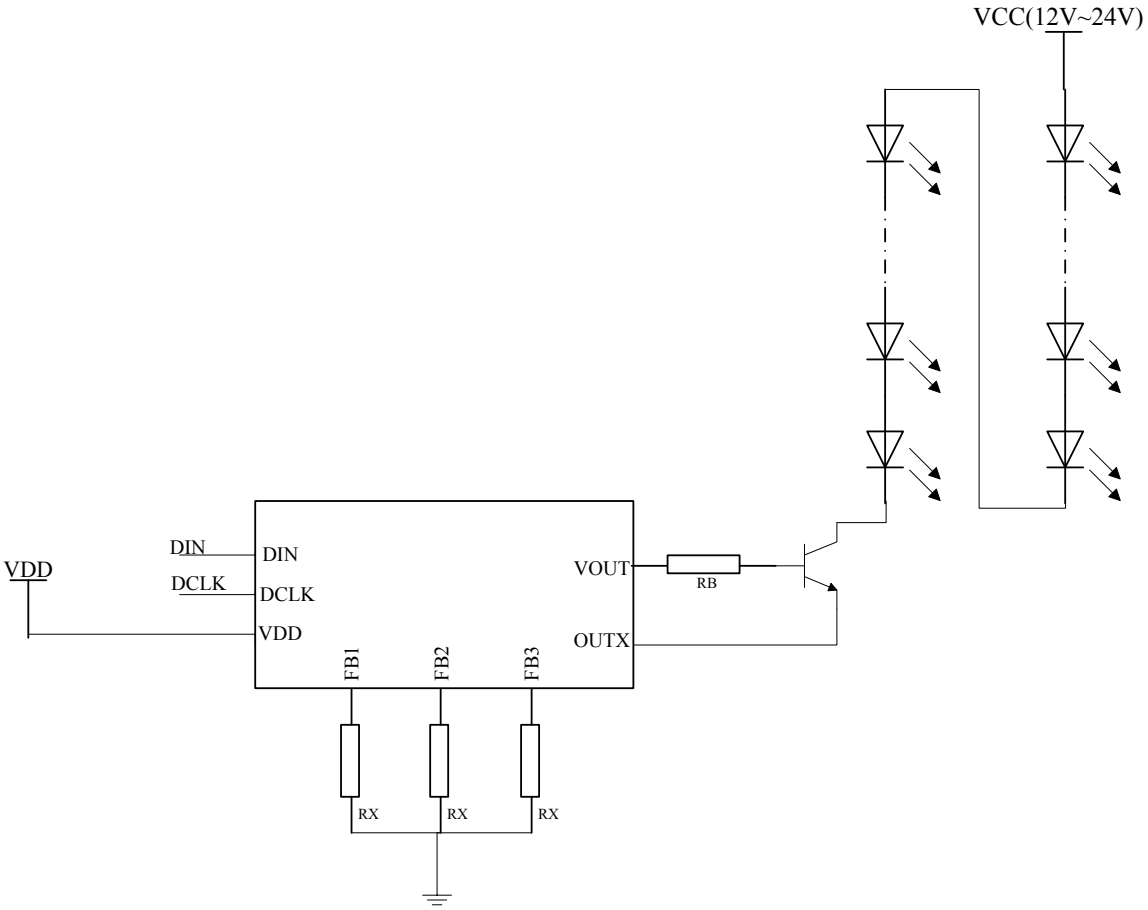
The current-limiting resistor is given by： RL = (VCC-V_{LED}-V_{CE})/20mA

The power tube is operated in the saturation zone, VCE is the saturation voltage drop of the power BJT, the value of which is normally 0.5~0.8V, the base resistor is 2K~5.1K, the connecting mode of other signals is the same with the fore mode.

This mode is usually applied in the connection method of series and parallel. In consideration of the situation that if one of the LED lamps is disconnected in the series branch, the whole LED lamps will be off. Therefore, the following principle should be obeyed in the connection method: the number of the series LED lamps in the branch should not be overmuch (normally 3~6 pcs), and the number of the parallel LED lamps in the branch should be more. The principle not only minimizes the influence of the failure caused by the burnout of a LED lamp, but also decentralizes the current-limiting resistor. By such

method, one high-power resistor is turned into multi low-power resistor, namely, the concentration installment is turned into decentralization installment; the single-set heat dissipation is improved and the design of the LED lamp can be conducted in a more compacted way.

- Plug-in Constant Current Driving Mode



This mode (OMODE=high level or opened) is suitable in the situation of cascading multi-LED lamps and a 12V+ VDD, the essence of which is to maintain the constant current driving characteristic of the circuit, and to improve the driving withstand voltage capacity through the external power BJT at the same time.

The current value that flows through the LED is given by: $I_{LED}=I_O*B/(1+B)$

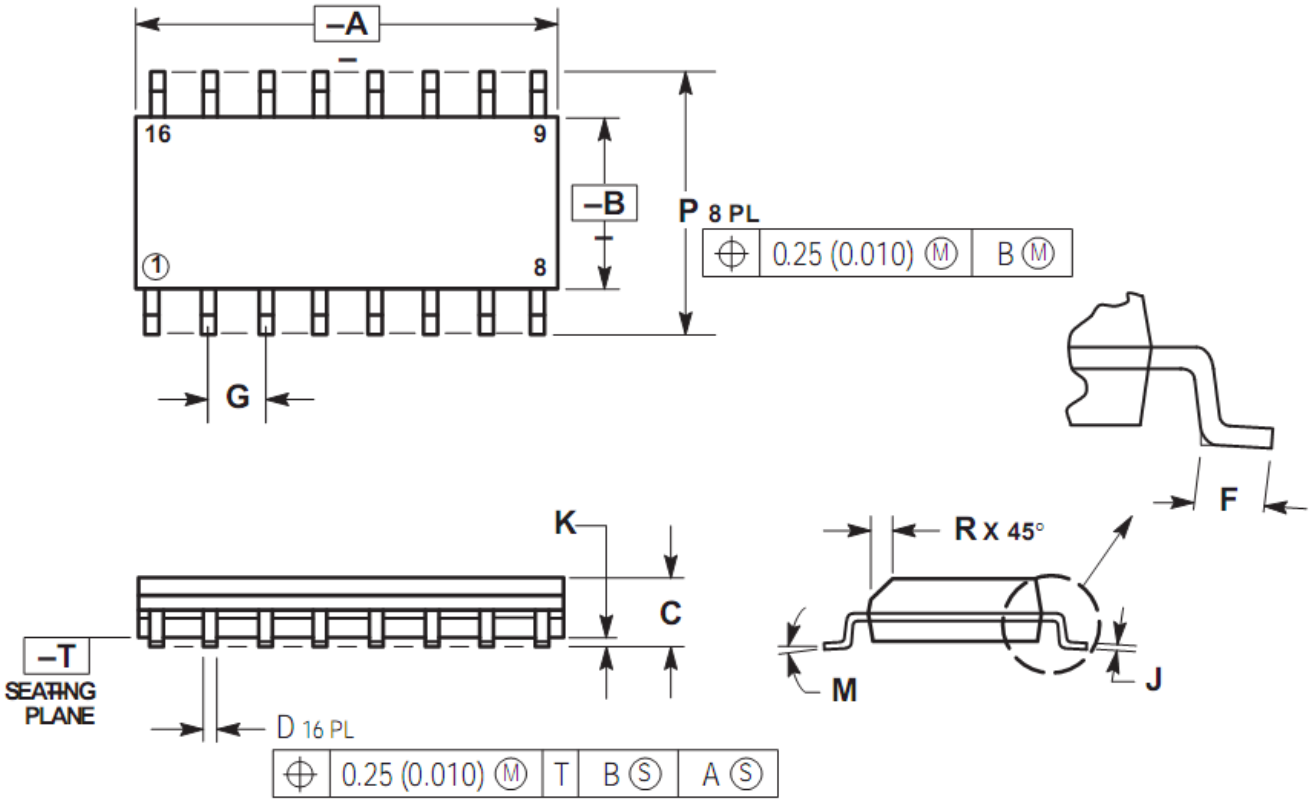
I_O is the current value corresponds to the RX in the chart 1, the power BJT is operated in the amplifier zone, B is the amplification times of the power BJT, when B is larger, and the above formula can be given approximately by:

$I_{LED}=I_O$ (the base resistor RB can be 5K)

The highest VCC voltage depends on the V_{CEO} of the NPN power BJT, the value of which is normally 25V+.

Package

SOP16



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.224
R	0.25	0.50	0.010	0.019