

SM16703SP

Feature

- ◆ Support input power voltage 2.5 ~ 26 V
- ◆ OUT R/G/B constant current value defaults to 18 mA
- ◆ OUT R/G/B power-on default state: open 50% duty cycle
- ◆ OUT R/G/B port withstand voltage : > 30 V
- ◆ OUT R/G/B output gray level: 256 levels
- ◆ Low standby power consumption: 210uA
- ◆ Synchronous refresh of display data in the same frame
- ◆ Using single-line return-to-zero code SID data protocol
- ◆ Data serial cascade transmission with strong anti-interference ability
- ◆ Signal transmission rate: 800Kbps
- ◆ Package form: SOP8

Application

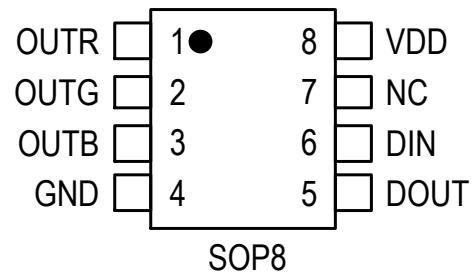
- ◆ Indoor LED decorative lighting
- ◆ Building exterior / scene lighting
- ◆ Point light source, perforated characters
- ◆ Soft light strips, linear lights

Description

SM16703SP is a single-line transmission three-channel LED drive control dedicated chip , using the single-line return-to-zero code SID data protocol .

SM16703SP supports a wide range of power supply, which can effectively improve the phenomenon of tail flicker caused by tail voltage attenuation. The default output current of the OUT R/G/B port is 18 mA. The application has the characteristics of few peripheral components of the chip, simplicity and reliability.

Pin diagram



Internal Function Diagram

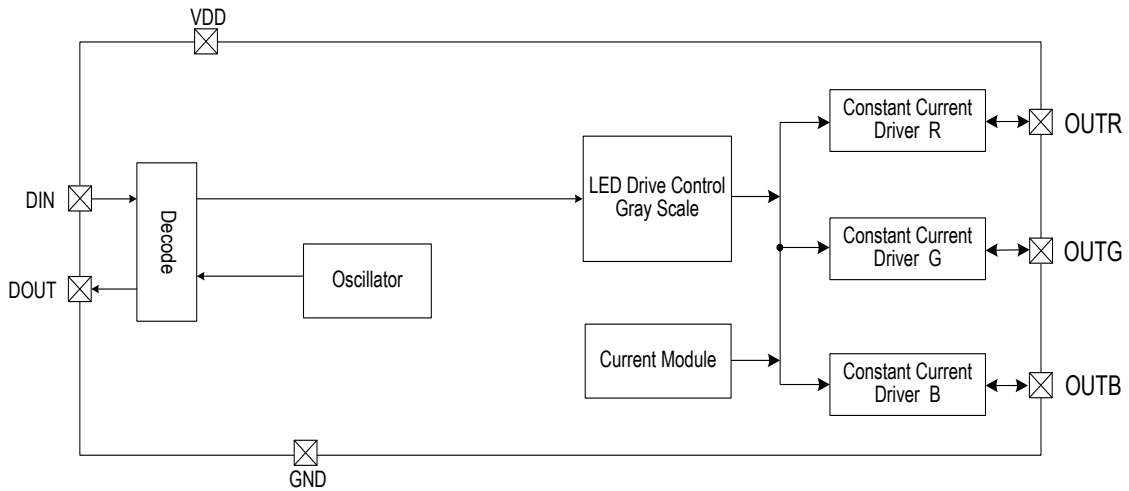


Fig . SM16703SP internal functional block diagram

Pin Description

Pin Name	Pin Description
OUTR	Constant current drive port
OUTG	Constant current drive port
OUTB	Constant current drive port
GND	Ground
DOUT	Cascaded signal output terminal
DIN	Signal input terminal
NC	No connection (users cannot connect to GND or VDD)
VDD	Power supply

Order Information

Type	Package	Packing		Reel size
		Tube	Tape	
SM16703SP	SOP8	100,000 pieces/box	4000 pieces/plate	13 inches

Absolute Maximum Parameter (Note 1,2,3)

Unless otherwise stated, $T_A = 25^\circ\text{C}$.

Symbol	Parameter	Range	Unit
V_{DD}	Operating Voltage	-0.4~+ 30.0	V
V_I	Logic input voltage	-0.4~+30.0	V
BV_{OUT}	OUT R/G/B breakdown voltage	30	V
$R_{\theta JA}$	Thermal resistance of PN junction to environment (Note 2)	130	$^\circ\text{C}/\text{W}$
P_D	Power consumption (Note 3)	0.5	W
T_J	Junction temperature of IC operation	-40~150	$^\circ\text{C}$
T_{stg}	Temperature of IC storage	-55~150	$^\circ\text{C}$
V_{HBM}	HBM ESD	± 2	KV

Note 1: The maximum output power is limited to chip junction temperature, the maximum limit means that the chip can be damaged beyond the range. The maximum limit value is work in the limit parameter range, the device function is normal, but it is not completely guaranteed to meet the individual performance indexes.

Note 2: $R_{\theta JA}$ was measured on a single-layer thermal conductivity test plate according to the JEDEC JESD51 thermal measurement standard under natural convection at $T_A=25^\circ\text{C}$.

Note 3: The maximum power consumption is determined by T_{JMAX} , $R_{\theta JA}$ and ambient temperature T_A . The maximum allowable power consumption is $P_D=(T_{JMAX}-T_A)/R_{\theta JA}$ or the lower value given in the limit range.

Electrical Operating Parameters (Note 4, 5)

Unless otherwise stated, $V_{DD}=5\text{V}$, $T_A=25^\circ\text{C}$.

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{DD}	Chip power supply voltage	-	2.5	-	26.0	V
I_{DD}	quiescent power consumption	I_{OUT} "OFF"	-	0.21	-	mA
$I_{OUT_R/G/B}$	R/G/B drive current	$V_{DS} = 1.5\text{V}$	-	18	-	mA
V_{IH}	Input signal threshold voltage	DIN input high level	2.6	-	-	V
V_{IL}		DIN input low level	-	-	1.4	V
I_{OH}	DOUT output current	DOUT output is high, connect $10\ \Omega$	-	8.5	-	mA
I_{OL}	DOUT sink current	DOUT output is low, short to VDD	-	18	-	mA
V_{DS_S}	OUT R/G/B constant current	$I_{OUT} = 18\text{mA}$	-	0.9	-	V
%VS. V_{DS}	OUT R/G/B current variable	$I_{OUT} = 18\text{mA}$, $V_{DS} = 1\sim 3\text{V}$	-0.3	-	+0.3	%
%VS. V_{DD}		$I_{OUT} = 18\text{mA}$, $V_{DD} = 3.3\sim 28\text{V}$	-0.5	-	+0.5	%
%VS. T_A		$I_{OUT} = 18\text{mA}$, $T_A = -40\sim +85^\circ\text{C}$	-5.0	-	+5.0	%
I_{leak}	OUT R/G/B port leakage	$V_{DS} = 47\text{V}$, I_{OUT} "OFF"	-	-	1	μA

Note 4: The electrical operating parameters define the DC parameters of the device within the working range and under test conditions that ensure a specific performance indicator. The specification does not guarantee the accuracy of the parameters that are not given the upper and lower limit values, but the typical values reflect the performance of the device.

Note 5: The minimum and maximum parameter range of the datasheet is guaranteed by the test, and the typical value is guaranteed by design, test or statistical analysis.

Switching Characteristic (Note 6,7,8)

Unless otherwise stated, $V_{DD}=5V$, $T_A=25^{\circ}C$.

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
f_{PWM}	OUT R/G/B output PWM frequency	$I_{OUT}=18mA$, OUT port connects 200 Ω resistor to VDD	-	4.7	-	KHz
t_{PLH}	Signal transmission delay (Note 6)	DOUT load capacitor to ground: 30pF, DIN to DOUT signal: transmission delay	-	-	90	ns
t_{PHL}			-	-	90	ns
t_{TLH}	DOUT transfer time (Note 7)	DOUT load capacitor to ground: 30pF	-	20	-	ns
t_{THL}			-	20	-	ns
t_r	OUT R/G/B transfer time (Note 8)	$I_{OUT}=9mA$, OUT R/G/B connects 200 Ω resistor to VDD, load capacitor to ground: 15pF	-	772	-	ns
t_f			-	660	-	ns

Note 6, Note 7, Note 8: As shown in the following figure.

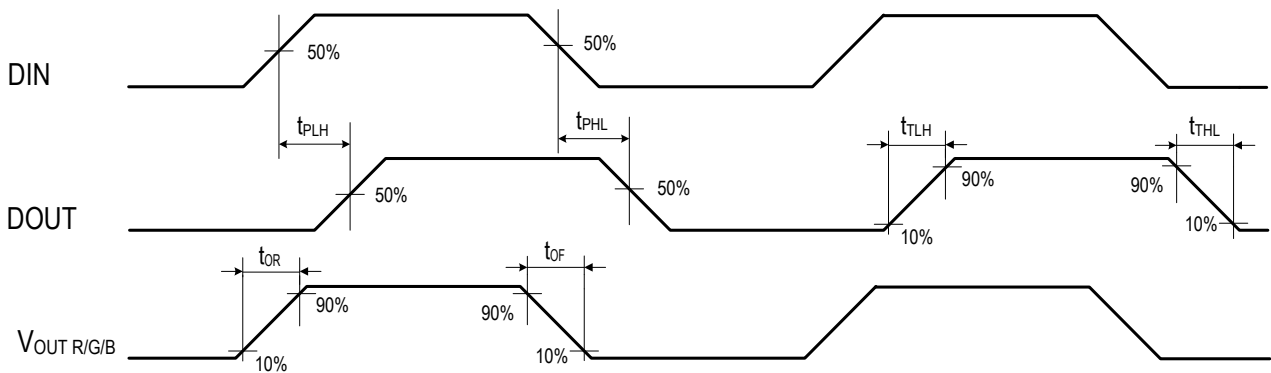


Fig. SM16703SP dynamic parameter test diagram

Data Communication Protocol (Note 9)

1. Code Description

The protocol of chip adopts single polarity RZ code, low level must be contained in each code element. Each code element in this protocol starts at a high level, the width of the high level time determines 0 code or 1 code.

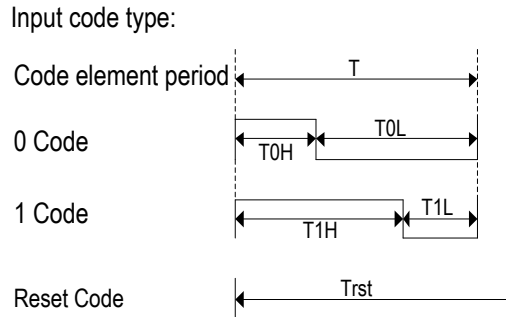


Fig. SM16703SP3 RZ code data communication protocol diagram

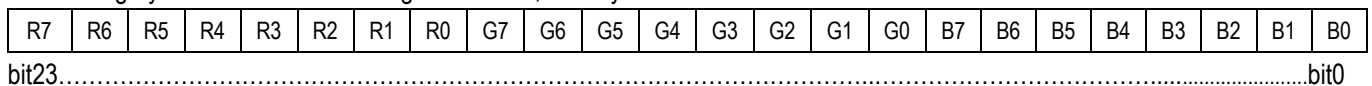
Symbol	Parameter	Min.	Typ.	Max.	Unit
T	Code element period	900	1200	20000	ns
T0H	0, HIGH level	200	300	400	ns
T0L	0, LOW level	700	900	-	ns
T1H	1, HIGH level	700	900	-	ns
T1L	1, LOW level	200	300	-	ns
Trst	Reset, LOW level	200	-	-	us

Note 9: The high-level time of 0 and 1 code should be in accordance with the specified scope of the above table, and the low-level time of 0 and 1 code is less than 100us.

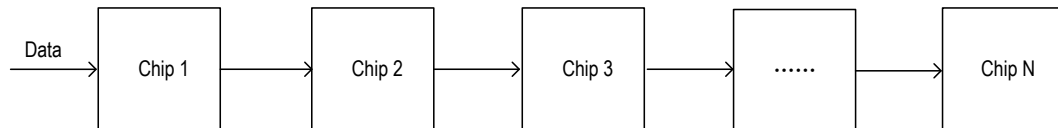
2. Protocol Data Format:

Trst+ First chip 24bits data +Second chip 24bits data +.....+ The N chip 24bits data +Trst

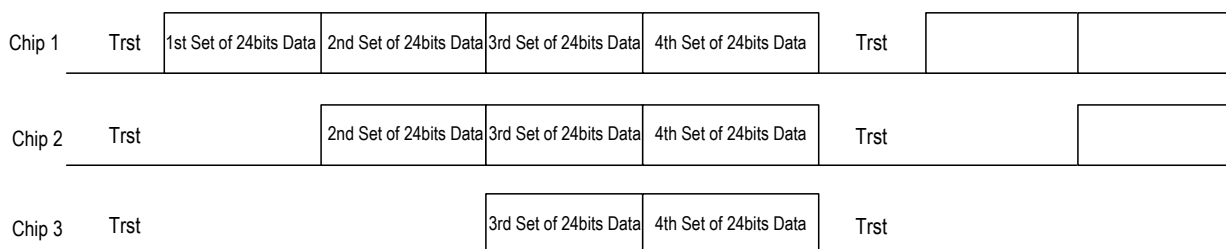
- 24bits gray scale data structure: High levels first, sent by the order of RGB



- System Topological Graph:



- Input Data Stream of every chip (3 chips as an example):



Constant Current Characteristics

After reaching the constant current inflection point, the SM16703SP output current is not affected by the OUT port voltage V_{DS} .

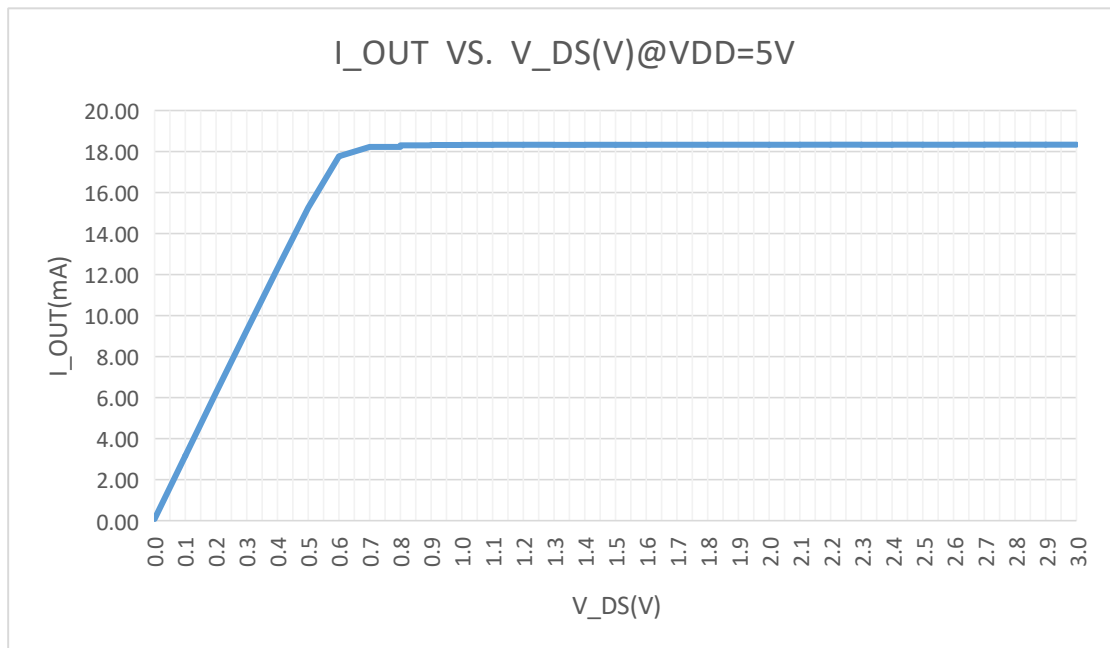


Fig. SM16703SP Relationship diagram between I_{OUT} and OUT port voltage V_{DS}

Typical Application Circuit

SM16703SP RGB solution typical application circuit diagram:

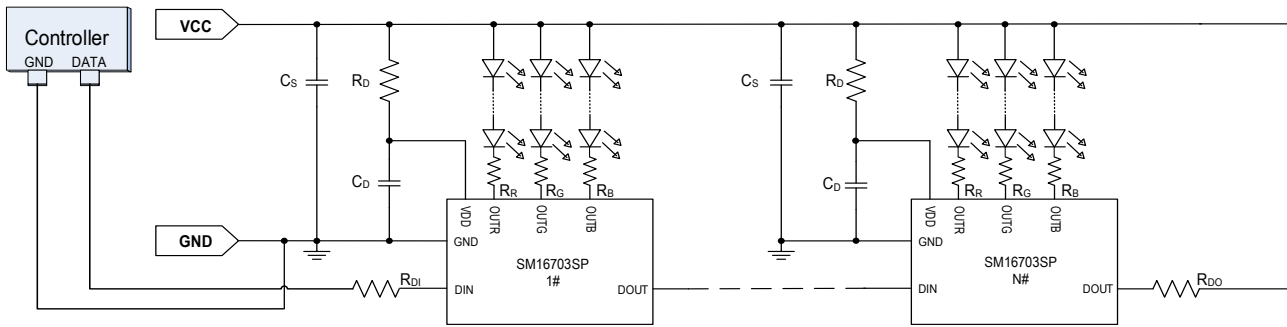


Fig. SM16703SP typical application scheme diagram

SM16703SP typical application circuit parameters include external input voltage V_{CC} , chip current limiting resistor R_D , LED voltage dividing resistor $R_R/R_G/R_B$, first chip DIN signal input port series resistor R_{DI} , tail end chip DOUT signal The output port is connected in series with resistor R_{DO} .

(1) V_{CC} is the external input voltage, and R_D is the current limiting resistor, which is used to prevent chip damage caused by reverse connection of the positive and negative poles of the power supply. Chip operating voltage $V_{DD} = V_{CC} - I_{DD} \times R_D$, where I_{DD} is the chip's quiescent current, and the R_D resistance must ensure that the reverse current is less than 80mA. The larger the R_D resistance, the stronger the anti-reverse connection ability; the smaller the R_D resistance, the greater the power consumption and the higher the operating temperature when the positive and negative poles of the power supply are reverse connected. The resistor R_D needs to be reasonably selected according to the system application environment during design. For different input power supply voltages V_{CC} , the design reference values of the current limiting resistor R_D are as follows:

$V_{CC}(V)$	5	9	12	15	18	twenty four
$R_D(\Omega)$	100	180	510	620	820	1K_

(2) C_S is the capacitance of the system power supply to the ground, which is used to reduce power supply fluctuations. A 0.1uF~10uF capacitor can be selected according to the actual load of the system. When the load is large, it is recommended to select an electrolytic capacitor. It can be omitted according to the actual application situation. capacitance;

(3) C_D is the chip filter capacitor, which is used to stabilize the VDD voltage of the chip and ensure the normal operation of the chip. The recommended value of C_D is a 100nF capacitor. Depending on the actual application, the capacitor can be omitted;

(4) R_{DI} is the first chip DIN signal input port protection resistor to prevent damage to the signal input port caused by hot plugging and hot plugging, reverse connection of the positive and negative poles of the power supply and the signal line, etc.;

(5) R_{DO} is the protection resistor for the DOUT signal output port of the tail-end chip to prevent damage to the signal output port caused by hot plugging, reverse connection of the positive and negative poles of the power supply and the signal line. This resistor affects the length of the signal cascade, and can be determined according to the actual situation. Make adjustments to the situation;

(6) $R_R/R_G/R_B$ is the voltage dividing resistor of the OUTR/G/B port, which is used to reduce the voltage of the OUTR/G/B port and reduce the chip power consumption.

The calculation formula is $R_R/R_G/R_B(\Omega) = (V_{CC} - V_{DS} - N \times V_{LED}) / I_{OUT}$, where V_{CC} is the external input voltage, V_{LED} is the voltage drop of the LED lamp, I_{OUT} is the port output current, V_{DS} is the OUTR port voltage. In practical applications, it should be ensured that the value of V_{DS} is higher than the constant current inflection point voltage, and at the same time Make the chip produce

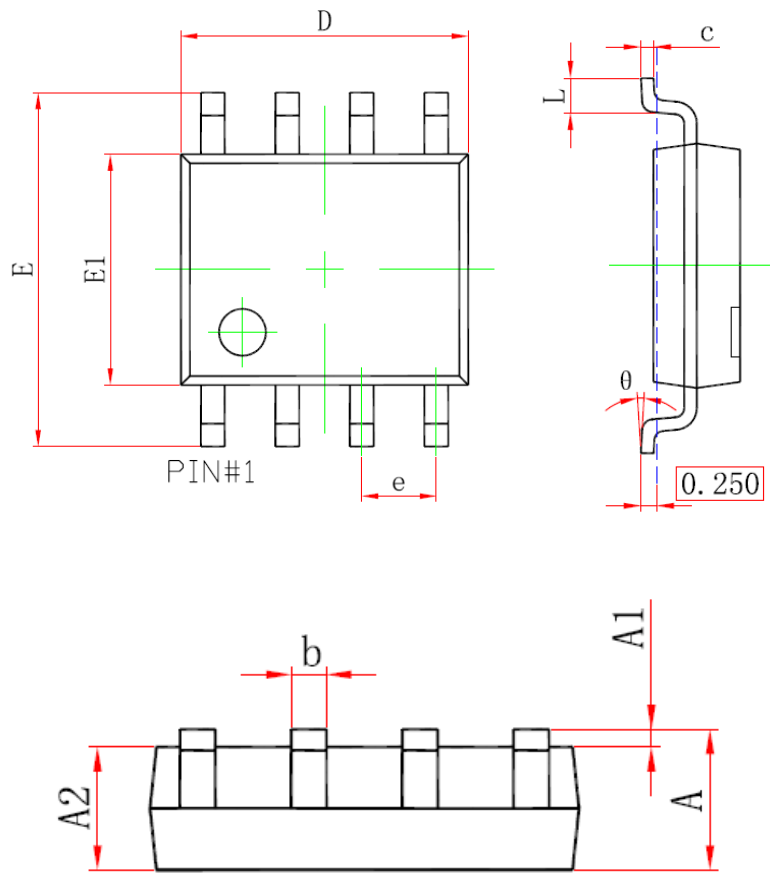
less power loss. The details are subject to actual application. The reference values of voltage drop V_{LED} for different color lamp beads are as follows: the voltage drop for red lamp is about 2.0~2.2V, and the voltage drop for green and blue lamp is about 3.0~3.2V. For details, please refer to the actual specifications of the lamp bead. shall prevail.

In typical applications, based on different input voltages and different numbers of lamp beads, the recommended values for each parameter are as follows:

VCC(V)	Number of LED serial connections to OUT port	$R_D(\Omega)$	$R_{DI}(\Omega)$	$R_{DO}(\Omega)$	$R_R(\Omega)$	$R_G(\Omega)$	$R_B(\Omega)$
12	3	510	120	120	200	-	-
24	6	1K	220	220	500	150	150

Package

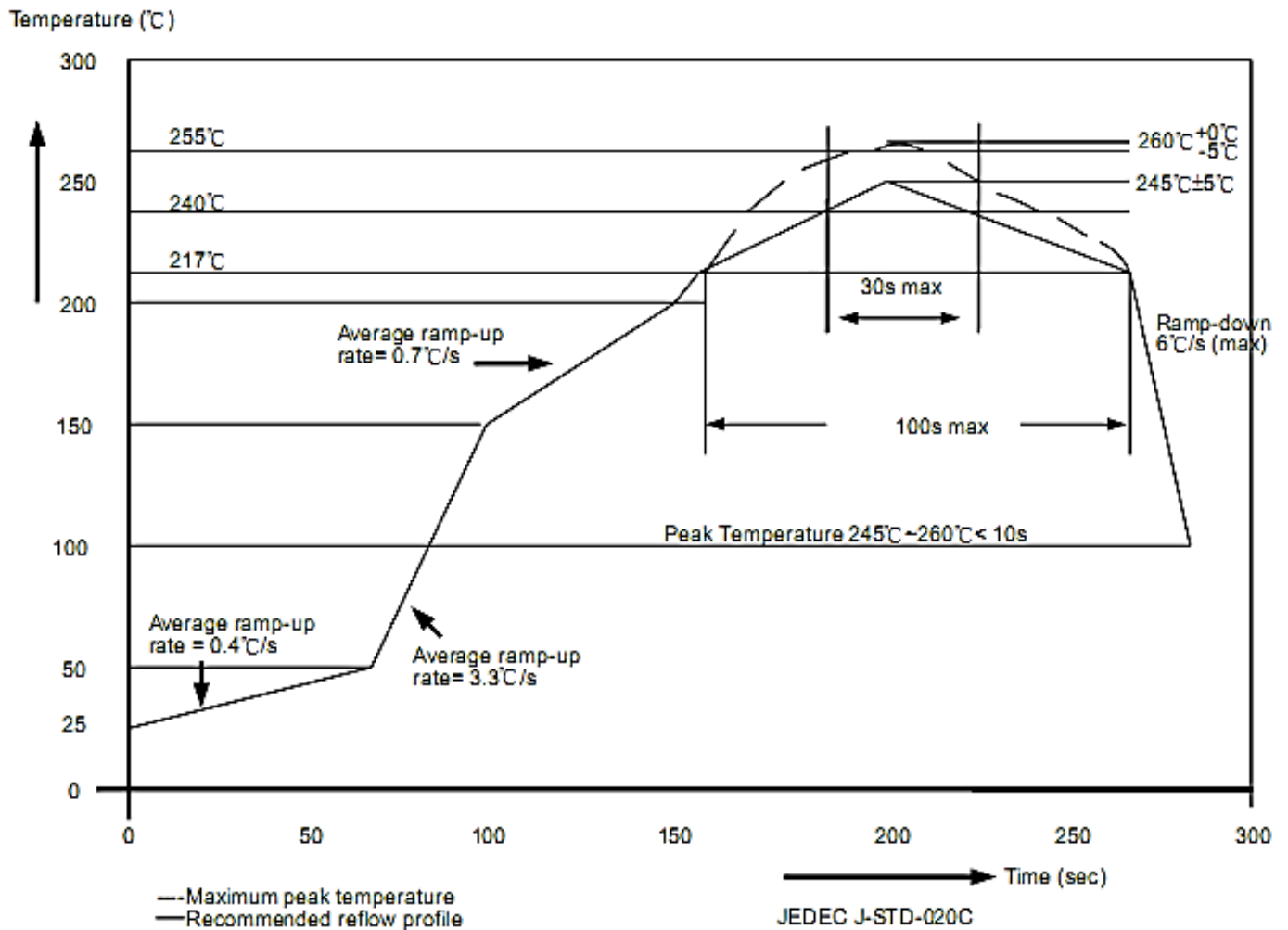
SOP8



Symbol	Min(mm)	Max(mm)
A	1.25	1.95
A1	-	0.25
A2	1.25	1.75
b	0.25	0.7
c	0.1	0.35
D	4.6	5.3
e	1.27(BSC)	
E	5.7	6.4
E1	3.7	4.2
L	0.2	1.5
θ	0°	10°

Encapsulation Soldering Process

Semiconductors of Sunmoon follow the European RoHs standard, solder temperature in encapsulation soldering process follows J-STD-020 standard.



Encapsulation Thickness	Volume mm ³ < 350	Volume mm ³ =350~2000	Volume mm ³ ≥ 2000
<1.6mm	260+0°C	260+0°C	260+0°C
1.6mm~2.5mm	260+0°C	250+0°C	245+0°C
≥2.5mm	250+0°C	245+0°C	245+0°C

Revision Record

Date	Revision	Revision Contents
2023-05-09	ZIZZQZVV1.0	First edition
2024-01-10	ZIZZQZAV1.0	Modify limit parameters V_{HEM}

Declaration

Sunmoon owns the right of alteration, correction, modification, improvement and termination about our products, files and services. To the rights above, recommend customers to contact our business representative for the latest product information before purchasing.

All technical applications need to be designed in strict accordance with the latest product specifications.

Sunmoon electronic products cannot be used in medical or military areas without our legal authorization. If users get injured or life threat even to dead, we are not responsible for any damage.

All verbal content, pictures and trademark are intellectual property of Sunmoon. Any individuals and organizations cannot use, correct, redo, public, remake, spread, publish or vend it to damage the legitimate rights and interests of Sunmoon, For the relevant infringement, we will immediately start a full legal process, held accountable.