

# SM16703P

## Feature

- ◆ Built-in power clamp, input power supply voltage 5~24V
- ◆ OUT R/G/B constant current value default 17mA
- ◆ OUT R/G/B power-on default state: bright white light
- ◆ OUT R/G/B port withstand voltage 26V
- ◆ OUT R/G/B output gray level: 256 levels
- ◆ Display data synchronization refresh in the same frame
- ◆ Unipolar return-to-zero code data protocol
- ◆ Cascaded data shaping output to prevent data attenuation
- ◆ Signal transmission speed: 800Kbps
- ◆ Package: SOP8

## Application

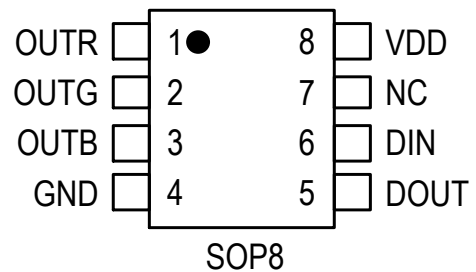
- ◆ Interior LED decorative lighting
- ◆ Architectural LED exterior/scene lighting
- ◆ Pointolite, punch word
- ◆ Soft light strip, line light

## Description

The SM16703P is a single-line transmission tri-channel LED driver, which adopts single-polarity RZ code SID data protocol.

The SM16703P default output current of the OUT R/G/B port is 17mA. The peripheral components of the chip are few, simple and reliable.

## Pin Definition



## Internal Function Diagram

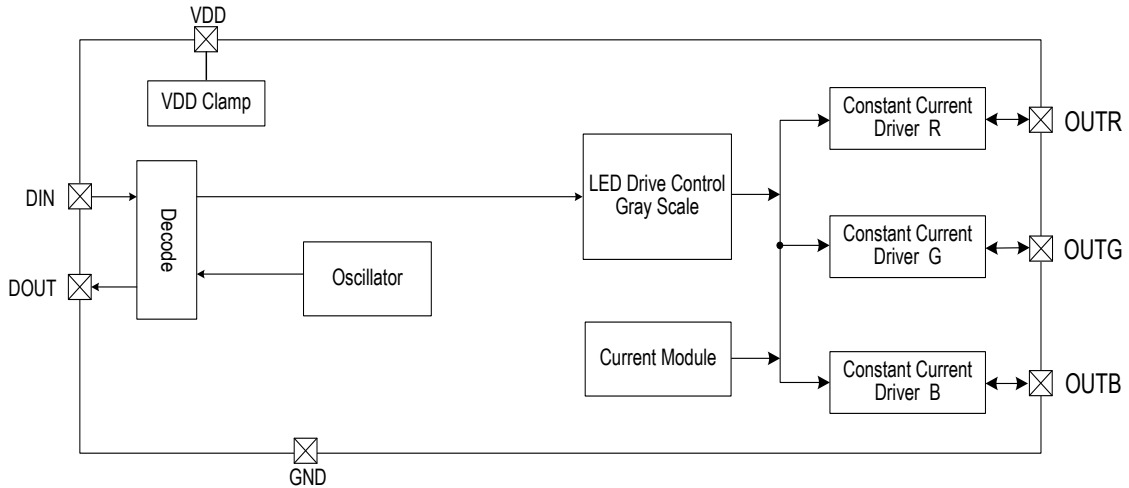


Fig. SM16703P internal function diagram

## Pin Definition

Pin No.	Pin Name	Pin Description
1	OUTR	Constant current drive port
2	OUTG	Constant current drive port
3	OUTB	Constant current drive port
4	GND	Ground
5	DOUT	Cascaded signal output port
6	DIN	Signal input port
7	NC	No connection (cannot connect to GND or VDD)
8	VDD	Chip power port

## Order Information

Type	Package	Packing		Reel Size
		Tube	Tape	
SM16703P	SOP8	100000 pcs/box	4000 pcs/tape	13 inches

## Absolute Maximum Parameter

Unless otherwise stated, Ta = 25°C.

Symbol	Parameter	Range	Unit
VDD	Chip operation voltage	-0.4~5.4	V
Vi	Logic Input voltage	-0.4~VDD+0.4	V
BV <sub>OUT</sub>	OUT R/G/B withstand voltage	30	V
I <sub>OUT</sub>	OUT R/G/B output current	18	mA
R <sub>θJA</sub>	Thermal Resistance Junction-to-Ambient(Note 2)	130	°C/W
P <sub>D</sub>	Power Dissipation(Note 3)	0.5	W
T <sub>J</sub>	Operating junction temperature	-40~150	°C
T <sub>STG</sub>	Storage temperature range	-55~150	°C
V <sub>ESD</sub>	HBM ESD	2	KV

Note 1: The maximum output power is limited to chip junction temperature, the maximum limit means that the chip can be damaged beyond the scope of the work. The maximum limit value is the work in the limit parameter range, the device function is normal, but it is not completely guaranteed to meet the individual performance indexes.

Note 2: R<sub>θJA</sub> measures the flow of water according to the JEDEC JESD51 thermal measurement standard on the single-layer thermal conductivity test board under TA=25°C.

Note 3: The maximum power consumption is decreased when temperature rising, this depends on T<sub>JMAX</sub>, R<sub>θJA</sub> and TA Maximum allowable power consumption is  $P_D = (T_{JMAX} - T_A) / R_{\theta JA}$  or the lower value of the value given in the limit range.

## Electrical Operating Parameter (Note 4, 5)

Unless otherwise stated, VDD=5V, TA=25°C.

Symbol	Description	Test Conditions	Min.	Typ.	Max.	Unit
VDD	Internal clamp voltage	VCC=12V, limited-resistor between VCC and VDD is $R_D=1K\Omega$	4.8	5.2	5.5	V
I <sub>DD</sub>	Quiescent Current	VDD = 4.5V, I <sub>OUT</sub> "OFF"	-	0.7	-	mA
V <sub>IH</sub>	Input signal threshold voltage	DIN input high level	0.7xVDD	-	-	V
V <sub>IL</sub>		DIN input low level	-	-	0.3xVDD	V
I <sub>OH</sub>	DOUT output current	DOUT output high level, serially connected 10Ω resistor to GND	-	-40	-	mA
I <sub>OL</sub>	DOUT sink current	DOUT output low level, the power supply sinks current to DOUT	-	40	-	mA
V <sub>DS,S</sub>	OUT R/G/B constant current knee point voltage	I <sub>OUT</sub> = 17mA	-	0.9	-	V
%VS.V <sub>DS</sub>	OUT R/G/B output current variation	I <sub>OUT</sub> = 17mA, V <sub>DS</sub> = 1.0~3.0V	-	0.5	-	%
%VS.VDD		I <sub>OUT</sub> = 17mA, VDD = 4.5~5.5V	-	0.5	-	%
%VS.TA		I <sub>OUT</sub> = 17mA, TA = -40~+85°C	-	4.0	-	%
I <sub>leak</sub>	OUT R/G/B Port leakage current	V <sub>DS</sub> = 26V, I <sub>OUT</sub> "OFF"	-	-	1	uA

Note 4: The electrical operating parameters define the DC/AC parameters of the device within the working range and under test conditions that ensure a specific performance indicator. The specification does not guarantee the accuracy of the parameters that are not given the upper and lower limit values, but the typical values reflect the performance of the device.

Note 5: The minimum and maximum parameter range of the datasheet is guaranteed by the test, and the typical value is guaranteed by design, test or statistical analysis.

## Switch Characteristic

Unless otherwise stated,  $V_{DD} = 5V$ ,  $T_A = 25^\circ C$ .

Symbol	Characteristic	Measurement Condition	Min.	Typ.	Max.	Unit
$f_{PWM}$	OUT R/G/B output PWM frequency	$I_{OUT} = 17mA$ , OUT series resistor $200\Omega$ to VDD	-	1.2	-	KHz
$t_{PLH}$	signal transmission delay (note 6)	DOUT port to ground load capacitance $30pF$ , Signal transmission delay from DIN to DOUT	-	85	-	ns
$t_{PHL}$			-	70	-	ns
$t_{TLH}$	DOUT transfer time (note 7)	DOUT port to ground load capacitance $30pF$	-	18	-	ns
$t_{THL}$			-	20	-	ns
$t_r$	OUT R/G/B transfer time (note 8)	$I_{OUT} = 17mA$ , OUT R/G/B series resistor $200\Omega$ to VDD, the load capacitance to ground is $15pF$	-	55	-	ns
$t_f$			-	75	-	ns

Note 6, Note 7, Note 8: as shown below:

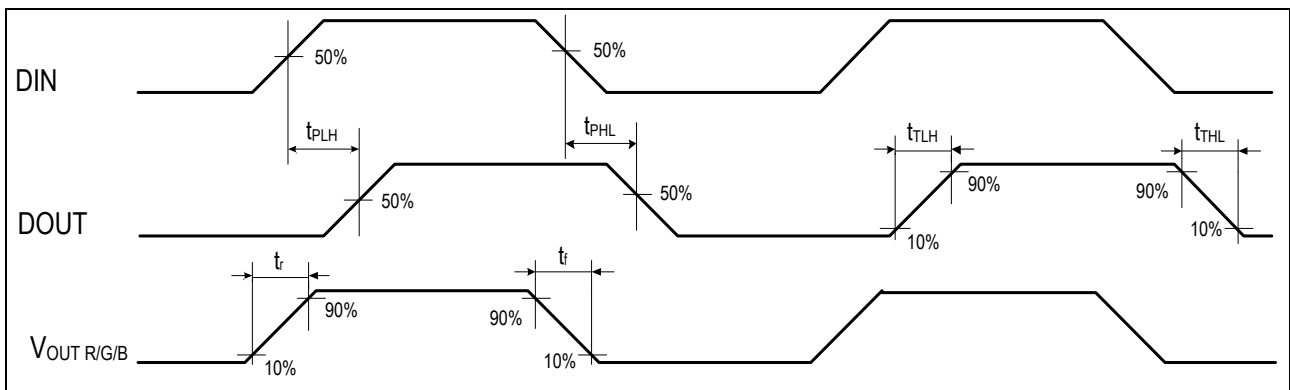


Fig. SM16703P Dynamic parameter test schematic

## Data communication protocol (Note 9, 10)

### 1、Code Description

The protocol of the chip adopts single polarity RZ code, LOW level must be contained in each code element. Each code element in the protocol initiates with HIGH level, and the width of the HIGH level time determines 0 code or 1 code.

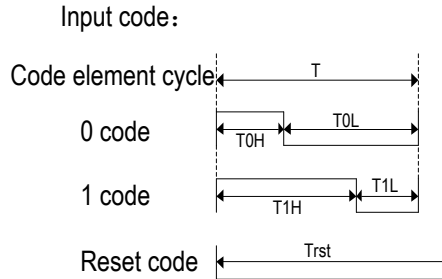


Fig. SM16703P RZ code data communication protocol diagram

Symbol	Description	Min.	Typ.	Max.	Unit
T	Code element cycle	1200	-	-	ns
T0H	0, HIGH level time	200	300	400	ns
T0L	0, LOW level time	800	900	-	ns
T1H	1, HIGH level time	800	900	1000	ns
T1L	1, LOW level time	200	300	-	ns
Trst	Reset code, LOW level time	200	-	-	us

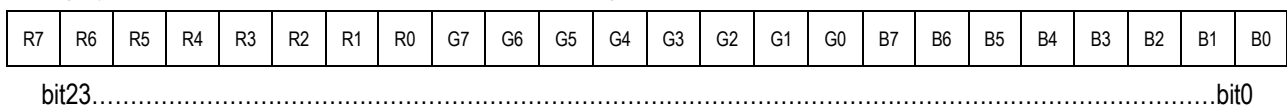
Note 9: When writing a program, the minimum symbol period requirement is 1.2us;

Note 10: 0 code, 1 code high time should be in accordance with the scope specified in the above table, 0 code, 1 code low time requirement is less than 20us;

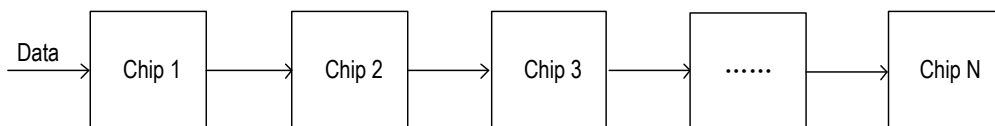
### 2、Protocol data format

Trst+ first chip 24bits data + second chip 24bits data +... + Nth chip 24bits data + Trst

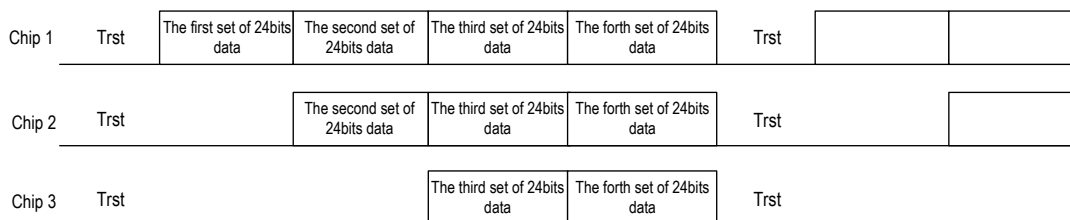
- 24bit grayscale data structure: RGB data transmission in high-order:



- System topology diagram:



Input data stream for each chip (take 3 chips as an example):



## Constant current characteristic

After reaching the constant current inflection point, the SM16703P output current is not affected by the OUT port voltage  $V_{DS}$ .

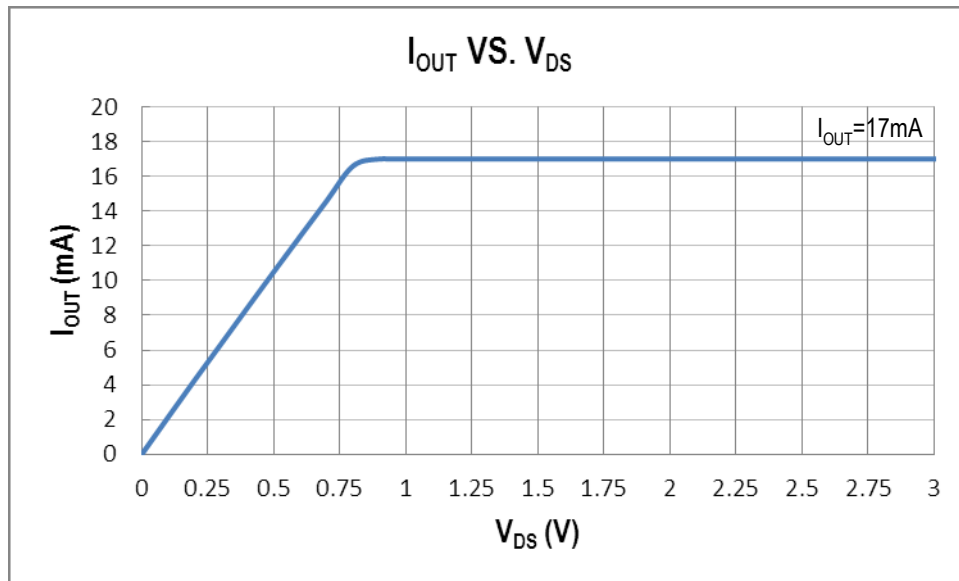


Fig. SM16703P diagram between  $I_{OUT}$  and voltage  $V_{DS}$  in OUT port

## Typical Application

SM16703P RGB typical application diagram

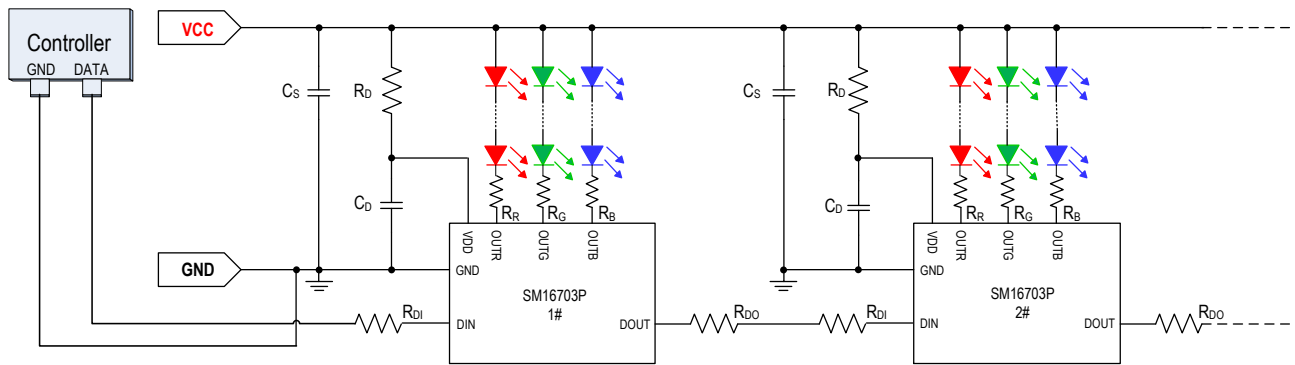


Fig. SM16703P typical application diagram

The typical application circuit of SM16703P includes input voltage of power supply VCC, system power filtering capacitor CS, chip current-limiting resistor RD, filter capacitor of chip VDD CD and R/G/B LED current-limiting resistors RR, RG, RB, DIN signal input port series resistor RDI and DOUT signal output port series resistor RDO.

(1) VCC is input voltage of power supply, RD is current-limiting resistor to limit the operating current of the internal voltage regulator module when the chip voltage regulator function is turned on. Chip operation voltage:  $VDD = VCC - I_{DD} \times R_D$ , I<sub>DD</sub> is the chip quiescent current, the value of RD must guarantee that VDD > 3V. The larger the RD resistance is, the lower the system power consumption is, but the system anti-interference ability is weak; the smaller the RD resistance is, the larger the system power consumption is, and the higher the operating temperature is. The design needs to select the resistor RD according to the system application environment. The design reference values of different input power supply voltages VCC and current limiting resistor RD are as follows:

VCC(V)	5	6	9	12	15	18	24
RD(Ω)	33	100	470	1K	1.5K	2K	3K

(2) CS is system power capacitance to the ground for reducing the power fluctuations, select 0.1uF-10uF according to actual load situation. Recommend to choose electrolytic capacitor when the load is bigger.

(3) CD is chip filter capacitor for keeping VDD voltage stable and guarantee normal operation. Recommend 100nF.

(4) RDI is the DIN signal input port protection resistor to prevent the signal port from being damaged due to the hot plugging, the positive and negative poles of the power supply and the reverse connection of the signal line;

(5) RDO is the DIN signal output port protection resistor to prevent the signal port from being damaged due to the hot plugging, the positive and negative poles of the power supply and the reverse connection of the signal line;

(6) RR, RG and RB are voltage divider resistors for the OTR/G/B ports, respectively, which are used to reduce the OTR/G/B port voltage and reduce the power consumption of the chip.

Its calculation formula is  $R_R / R_G / R_B (\Omega) = \frac{VCC - V_{DS} - N \times V_{LED}}{I_{OUT}}$ , VCC is the external input voltage, V<sub>LED</sub> is the LED lamp

voltage drop, I<sub>OUT</sub> is the port output current, V<sub>DS</sub> is the chip OTR/G/B port voltage, in practical applications, the V<sub>DS</sub> value should be higher than the constant current knee point voltage, and at the same time the chip produces less power loss. The actual application is



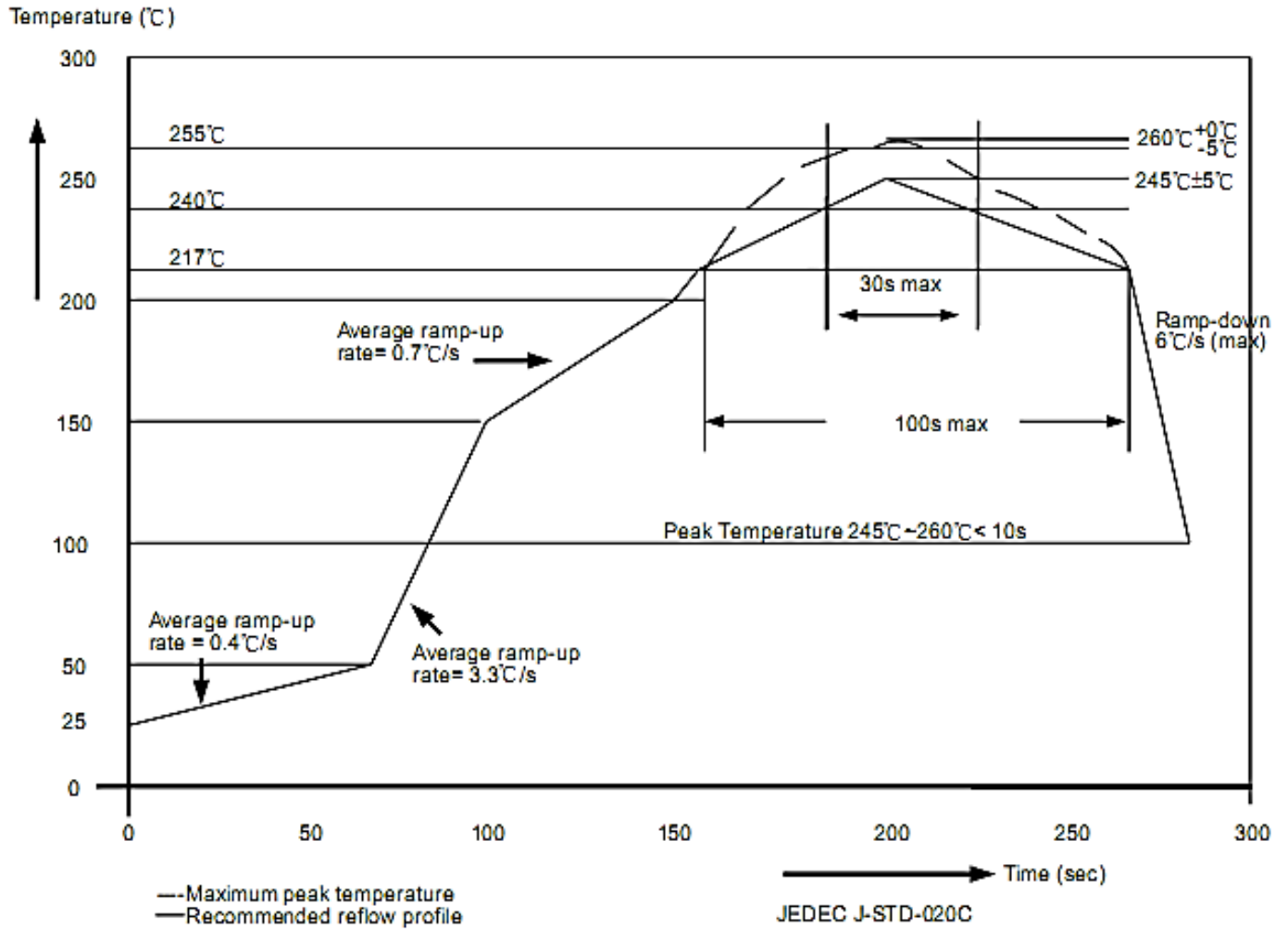
subject to the standard. The reference value of the voltage drop  $V_{LED}$  of different colors is as follows: the red lamp voltage drop is about 2.0~2.2V, and the green, blue and white lamp voltage drop is about 3.0~3.2V. Please refer to the actual lamp bead.

In a typical application, according to different input voltages and different number of lamp beads, the corresponding values of the corresponding parameters are as follows:

VCC(V)	OUT port series number of LED (CH)	$R_D(\Omega)$	$C_D(nF)$	$R_{DI}(\Omega)$	$R_{DO}(\Omega)$	$R_R(\Omega)$	$R_G(\Omega)$	$R_B(\Omega)$
12	3	1K	100	51	150	150	-	-
24	6	3K	100	100	300	510	150	150

## Encapsulation Soldering Process

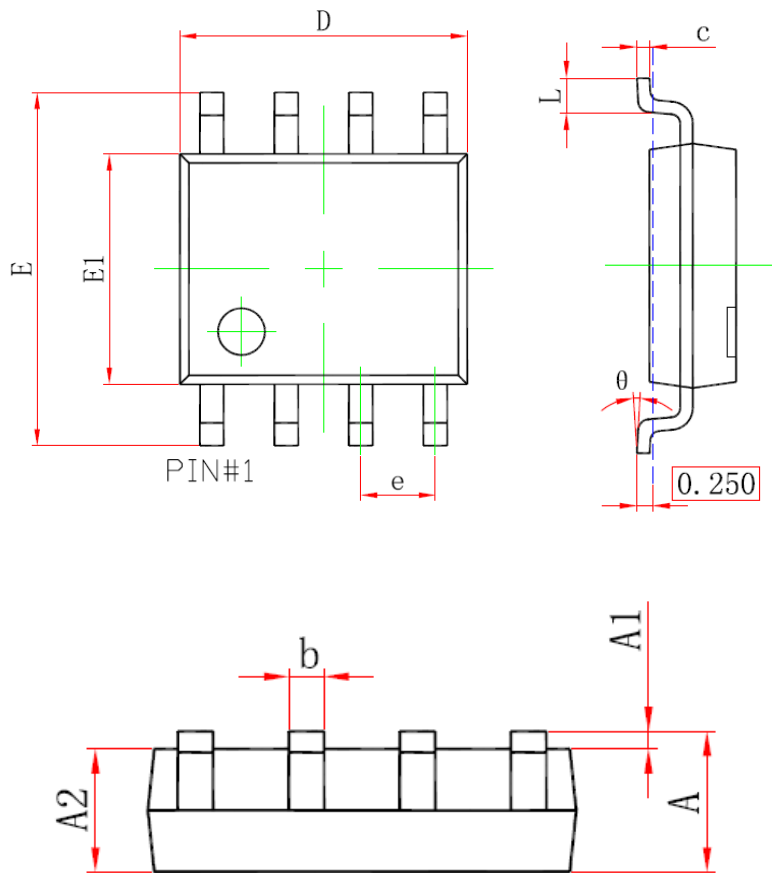
Semiconductors of Sunmoon follow the European RoHs standard, solder temperature in encapsulation soldering process follows J-STD-020 standard.



Encapsulation Thickness	Volume		
	mm <sup>3</sup> < 350	mm <sup>3</sup> : 350-2000	mm <sup>3</sup> ≥ 2000
<1.6mm	260+0°C	260+0°C	260+0°C
1.6mm-2.5mm	260+0°C	250+0°C	245+0°C
≥2.5mm	250+0°C	245+0°C	245+0°C

## Package

SOP8



Symbol	Min(mm)	Max(mm)
A	1.25	1.95
A1	-	0.25
A2	1.25	1.75
b	0.25	0.7
c	0.1	0.35
D	4.6	5.3
e	1.27(BSC)	
E	5.7	6.4
E1	3.7	4.2
L	0.2	1.5
$\theta$	0°	10°

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