Overview

LB1908 is a dedicated chip for LED constant current drive with 3 channels of return to 0 code that supports resumable transmission. There are 3 open-drain constant current output terminals, support 256-level brightness adjustment, PWM refresh rate up to 8K, and provide output channel current misalignment processing methods that reduce electromagnetic interference and power supply clutter. The IC is directly connected to the 12V power supply to reduce the impact of voltage drop; the chip provides dual data inputs as redundant control to ensure signal transmission in the case of single chip damage. The chip provides SOP8 package.

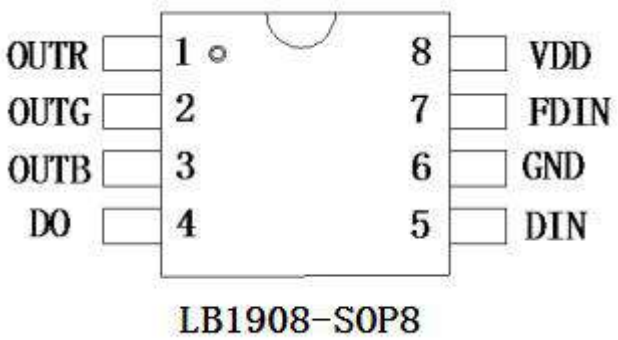
Applications

· LED Display
·LED lighting/light engineering

Features

- Using power CMOS technology, OUT output port withstand voltage 24V.
- Built-in 5V voltage regulator tube, working voltage 12V.
- Using return to 0 code, serial data transmission rate 800KHz.
- Fixed constant current output of 14mA, default does not turn on when power is on.
- PWM brightness control circuit, 256-level brightness adjustable; gray-scale clock supports 8KHZ refresh rate.
- Accurate current output value: (channel and channel) maximum error: ±3%, (chip and chip) maximum error: ±5%.
- Single-wire dual-channel serial cascading interface: switch between input interfaces in normal mode, DIN pin inputs data in DIN working mode, FDIN pin inputs data in FDIN working mode, D0 forwards cascaded data, and the signal does not depend on a certain one. The chip is abnormal and affects the normal operation of other chips.
- Oscillation mode: Built-in RC oscillation and clock synchronization according to the signal on the data line, after receiving the data of this unit, the subsequent data can be automatically regenerated and sent to the lower level through the data output terminal, and the signal will not be distorted or distorted as the cascade becomes farther. Attenuation.
- Built-in power-on reset circuit, all registers are initialized to zero after power-on reset.
- ESD:HBM 3000V MM 300V
- Packaging:SOP8(4000PCS/Reel)

Pin Configuration



LB1908-SOP8

Pin Description

PIN name	PIN NO.	I/O	Function
DIN	5	I	Data input
FDIN	7	I	Backup data input
DO	4	O	Data output
GND	6	--	Chip Ground
OUTR/G/B	1、2、3	O	Constant-current outputs，connected to LED
VDD	8	--	12V Power Supply

Integrated circuit is an electrostatic sensitive device which tends to generate a lot of static electricity when used in a dry season or dry environment. Electrostatic discharge may damage integrated circuit. Titan Micro Electronics suggests taking all appropriate preventive measures for integrated circuit. Improper operation and welding might cause ESD damage or performance reduction and chip operation failure.

Maximum Ratings

Parameter name	Parameter symbol	Limit value	Unit.
Power Source	VDD	-0.4～16	V
On-chip Power Source	VCC	-0.4～6	V
Input Logic Voltage	Vin	-0.4～VDD+0.5	V
Output voltage-endurance	Vout	26	V
Maximum output current	I_{OUT}	15	mA
Working temperature	Topr	-40～+85	℃
Storage temperature	Tstg	-50～+150	℃
ESD	Human body model (HBM)	3000	V
	Machine model (MM)	300	V

(1) When the chip works for a long time under the above limit parameters, it may cause device reliability reduction or permanent damage. We do not suggest the chip works by exceeding these limit parameters under any other conditions.
(2) All voltage values are comparatively tested in a systematic way.

Electrical characteristics

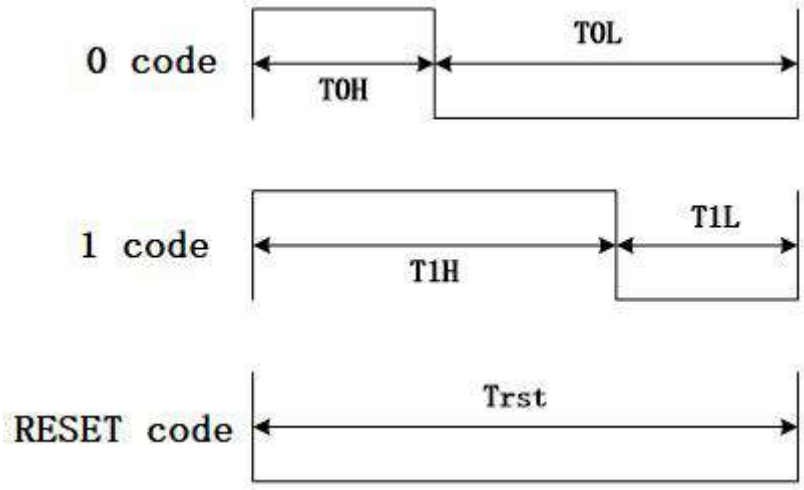
Parameter name	Parameter symbol	Testing condition	Min	Typical	Max	Unit
Power supply	*VDD*	Ioh=3mA	10	12	16	V
High Input Logic Voltage	Vih	VDD=5.0V	4		VDD	V
Low Input Logic Voltage	Vil	VDD=5.0V	0		1.0	V
Voltage range of outputs	Vout	OUT＝OFF			12	V
Static current	IDD	VDD=5.0V，GND=0V，其他端口悬空	0.5	1.4	2.0	mA
OUT output current	Iout	OUTR，OUTG，OUTB=ON，Vout=3.0V	9	10	11	mA
OUT output leakage current	Iolkg	OUTR，OUTG，OUTB=OFF，Vout=12.0V			0.5	μA
Current variation(channel)	ΔIolc0	OUTR，OUTG，OUTB=ON，Vout=3.0V			±3	%

Current variation(chip)	ΔIolc1	OUTR，OUTG，OUTB=ON，Vout=3.0V			±5	%
Power dissipation	Pd	Ta=25℃			150	mW
PWM refresh rate	Fin			800		KHz
OUT PWM refresh rate	Fout	OUTR，OUTG，OUTB		8K		Hz
Propagation delay time	Tplz	DIN → DO FDIN → DO		155	500	ns
External Power Res	Ri			50		ohm
External Power Cap	Ci			0.1		uF

Time sequence characteristics

Parameter name	Parameter symbol	Testing condition	Min	Typical	Max	Unit
Input 0 ode, high level time	T0H	VDD=5.0V GND=0V	250	300	350	ns
Input 1 ode, high level time	T1H		700	800	900	ns
Output 0 ode, high level time	T0H’			300		ns
Output 1 ode, high level time	T1H’			800		ns
0 code or 1 code cycle	T0/T1		1.1	1.2	1.3	μs
Reset code, low level time	Treset		200			μs

(1) When 0 code or 1 code cycle is within the range of 1.2μs (frequency 800KHz) , the chip can normally work, but the low level time of 0 code and 1 code must accord with the corresponding values in the above table;
(2) When reset is not required, the low level time between bytes should not exceed 80μs, or else the chip may be rest to receive data again, which cannot achieve correct data transmission.



Function description

1. Display data

LB1908 adopts single-wire two-channel communication and adopts 0-code mode to send signals.After power-on reset and reception of a mode setting command, the chip begins to receive display data. When the 24-bit data are received, DO ports will start to forward the data continuously sent from DIN or FDIN port, which provides display data for the next cascaded chip. Prior to forwarding data, DO ports are always at low level. If DIN or FDIN port is input with Reset signals, chip OUT port will output the PWM waveform of corresponding duty ratio according to the received

24-bit data, and the chip will wait to receive new data again.Upon receiving the initial 24-bit data, DO port will forward the data. Before the chip receives no Reset signal,the original output of OUTR, OUTG and OUTB remains unchanged.

The chip adopts auto integer forwarding technology, so that the signals will not distort and attenuate. For all the cascaded chips, the cycles of data transmission are consistent.

2. Structure of a complete frame of data

D1	D2	D3	D4	···	Dn	Reset	D1	D2	D3	D4	···	Dn	Reset

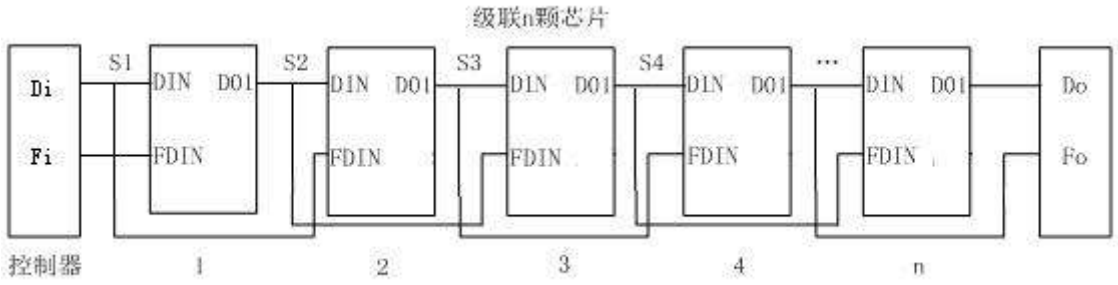
The data formats of D1, D2, D3, D4,…Dn are the same, wherein D1 means the display data packet of the first cascaded chip and Dn means the data display packet of the n_{th} cascaded chip. Each display data packet contains 24 data bits. Reset means reset signal, valid at low level.

3. Data format of Dn

R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0

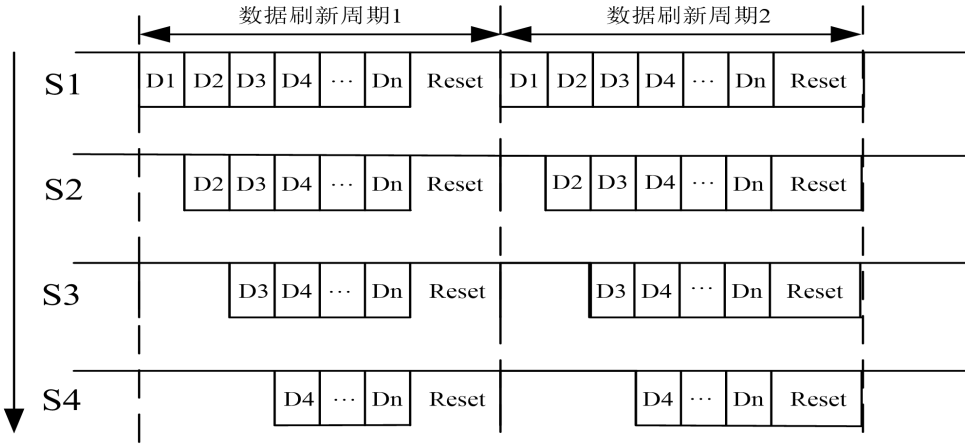
Each data packet contains 8×3 data bits, with higher bits sent first.
R[7:0]: used to set the PWM duty ratio output by OUTR. Full 0 code is off, full 1 code is of maximum duty ratio, 256-level adjustable.
G[7:0]: used to set the PWM duty ratio output by OUTG. Full 0 code is off, full 1 code is of maximum duty ratio, 256-level adjustable.
B[7:0]: used to set the PWM duty ratio output by OUTB. Full 0 code is off, full 1 code is of maximum duty ratio, 256-level adjustable.

4. Data reception and forwarding



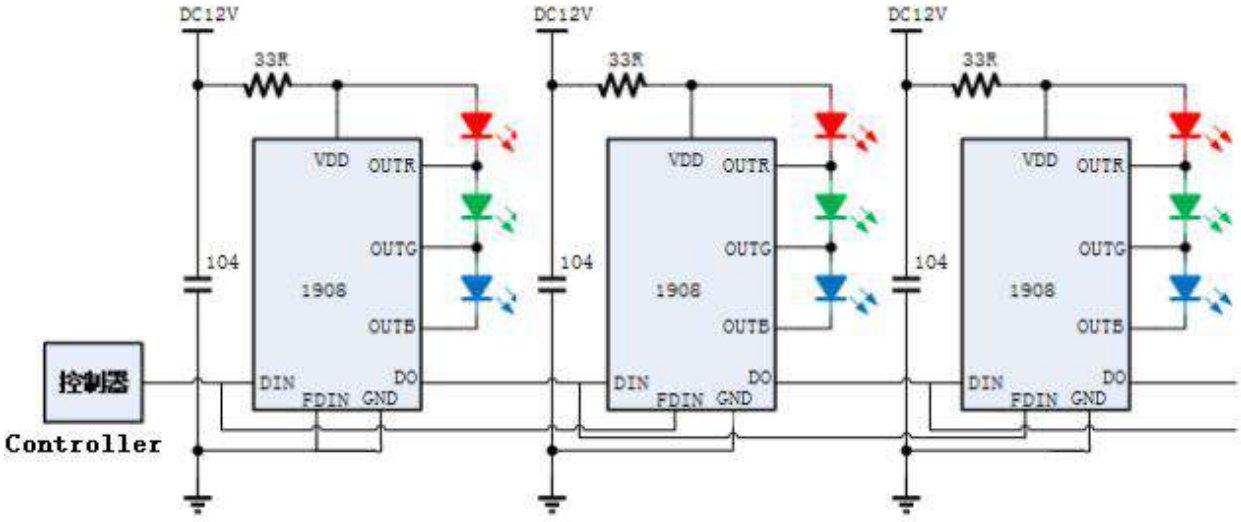
Special reminder: the IC PINS DIN and FDIN as two input of data is not the same, and exactly 24 bits of data, when FDIN received data, automatically lose the Dx that packet to achieve that data (display effect) will not shift, which is the first point to connect the controller using THE DIN port instead of the FDIN port.

Wherein, S1 is the data sent by Di port of the controller, S2, S3 and S4 are the data forwarded by cascaded LB1908.
Data structure of Di and Fi2 ports of the controller: D1D2D3D4……Dn;
Data structure of Fi port of the controller: DxD1D2D3……Dn; and the Dx is any 24bit data.



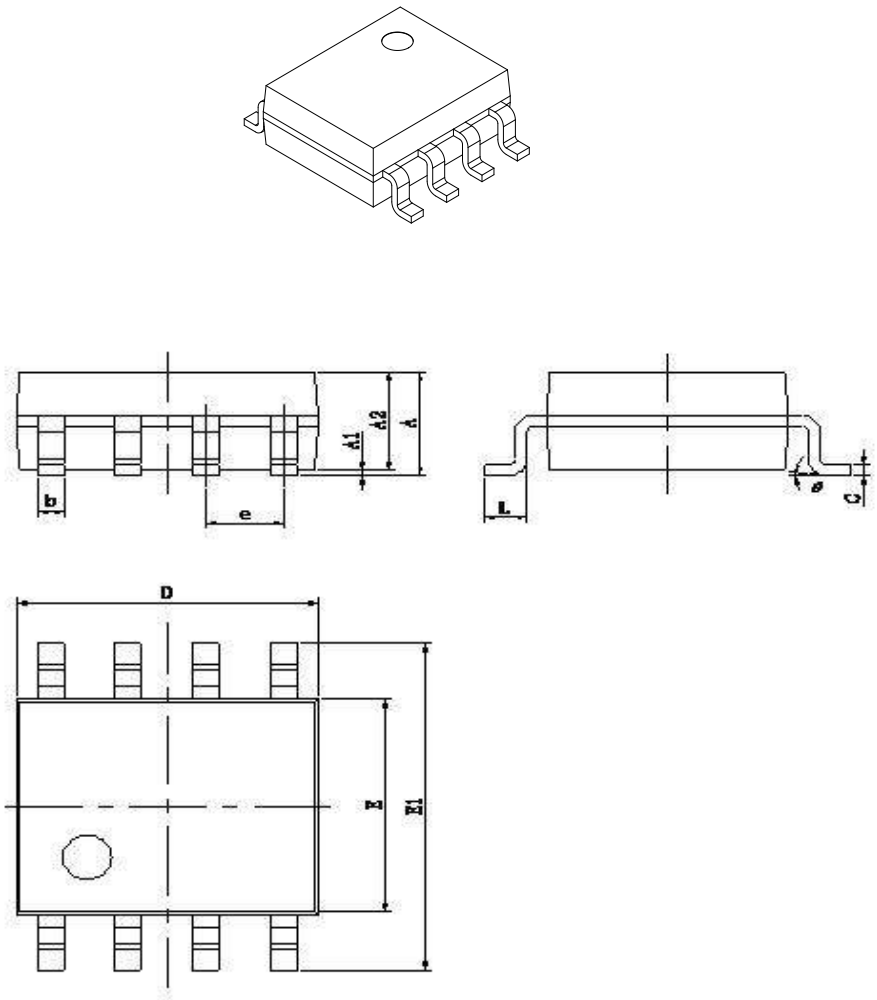
The data transmission and forwarding process when chips are cascaded is as follows: controller sends packetD1, Chip 1 receives the first set of 24bit,At this time, chip 1 has no forwarding;Then the controller sends the packet D2,Chip 1 receives the second set of 24 bits,Since the chip 1 already has the first set of 24 bits,Therefore, the chip 1 forwards the second group 24 bits to the chip 2 through the DO.The chip 2 receives the data packet D2 forwarded by the chip 1,At this time, chip 2 has no forwarding;The controller then sends the packet D3,Chip 1 forwards the received third set of 24 bits to chip 2,Since the chip 2 already has a second set of 24 bits,Therefore, the chip 2 forwards the third group 24bit to the chip 3, and the chip 3 receives the third group 24bit; and so forth, until the controller sends Reset signal, all the chips will reset and control the received 24-bit data to output them from OUT port after decoding, which completes a data refresh cycle and makes the chips return to the reception-ready state. Reset is valid at low level. To make the chip reset, the low level time should be maintained at more than 200μs.

Typical application circuit



To prevent chip signal input/output pin damage caused by the transient peak voltage generated by hot plugging when the product is tested, 68-100Ω protective resistors should be connected in parallel at signal input and output pins. Besides, the 104 decoupling capacitance of each chip in the figure is indispensable, and the wiring to the VDD and GND pins of the chips should be as short as possible, in order to achieve optimal decoupling effect and stable chip operation.
The first point controller only needs to be connected to the DIN port, and the FDIN port is grounded; in addition, if the breakpoint resume function is not required, all FDINs can be left floating. In addition, in order to reduce the thermal power consumption of the IC, a 33R resistor can be connected to the VDD port.

Packaging diagram (SOP 8)



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

(All specs and applications shown above subject to change without prior notice.)